REMARKS/ARGUMENTS

Claims 1-54 are pending in this application. Claims 1, 13, 16, 18, 33, 36, and 39-44 are amended. The specification is also amended to correct a typographical error. Claims 7, 8, 24, and 25 are allowed (page 17 of the Office action). However, on the cover sheet (PTO form L-326) box 7 (instead of box 5) is checked, indicating that claims 7, 8, 24, and 25 are objected to. A correction of the above mistake and clear indication of the allowance of these claims are respectfully requested.

Claims 1-3, 5, 10, 13-15, 18-19, 21-22, 27, 33-35, 39-40, 42-43, 45-46, 48-49, and 51-54 are rejected under 35 U.S.C. 102(b) as being anticipated by J. B. Rosenberg, "How debuggers Work: Algorithms, Data Structures, and Architecture," ("Rosenberg"). Claims 1-6, 9, 10, 18-23, 26-27, 39, 42, 45, 48, 48, 51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosenberg, in view of Deao et al. (US 6,112,298). Claims 11 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosenberg, in view of Deao and further in view of Wu (US 5,404,428). In view of the above amendments and following remarks, Applicants respectfully submit that the application is in condition for allowance, therefore, reconsideration and allowance of the application are respectfully requested.

Amended independent claims 1, 18, 39, and 42, include among other limitations "executing one or more instructions for recording old values of scalar registers, if the breakpoint is

set on an instruction that used the old values of the scalar registers," and "restoring the state of the executing service using the recorded old values of scalar registers."

Rosenberg does not teach or disclose the above limitation. Deao describes an emulation unit which allows debugging and emulation of an integrated circuit when connected to an external test system. The emulation unit provides means for emulating the unprotected pipeline of microprocessor to prevent extraneous operations from occurring which could otherwise affect memories or peripheral devices during emulation. (See, Summary of Invention and Abstract). A sequence of halts are inserted "in a procedure for stopping the pipeline and saving as a state the contents of various registers within the pipeline, referred to as a "pipe-down" procedure. Instructions in execute packets that have completed E1 (a-d) are allowed to proceed to completion." (Col. 49, lines 39-44).

Although, Deao mentions "stopping the pipeline and saving as a state the contents of various registers within the pipeline," this does not suggest "executing one or more instructions for recording old values of scalar registers, if the breakpoint is set on an instruction that used the old values of the scalar registers," as required by the independent claims 1, 18, 39, and 42. In fact, the system of Deao does not check to verify that "the breakpoint is set on an instruction that used the old values of the scalar registers." As a result, Deao does no teach or suggest the limitation of "executing one or more instructions for recording old values of scalar registers,

if the breakpoint is set on an instruction that used the old values of the scalar registers," as required by the independent claims 1, 18, 39, and 42.

Therefore, neither Rosenberg nor Deao, alone or in combination, discloses or suggests the above-recited limitation.

Applicants therefore respectfully submit that claims 1, 18, 39, and 42 are novel and unobvious over the cited references and are therefore allowable. Applicants further submit that dependent claims 2-6, 9-12,19-23, 26-32, 45 and 53 that depend directly or indirectly from claims 1, 18, 39, and 42, respectively are allowable as are claims 1, 18, 39, and 42, and for additional limitations recited therein.

Amended independent claims 16, 36, 41, and 44, include among other limitations "executing one or more instructions for recording old values of scalar registers, if the breakpoint is set on an instruction that used the old values of the scalar registers."

As discussed above, neither Rosenberg nor Deao, alone or in combination, discloses or suggests the above-recited limitation. Therefore independent claims 16, 36, 41, and 44 are also novel and unobvious over the cited references and are therefore allowable.

Dependent claims 17, 37-38, are dependent from independent claims 16, and 36, respectively and therefore include all the limitations of their respective independent claims and

additional limitations therein. Accordingly, these claims are also allowable over the cited references, as being dependent from allowable independent claims and for the additional limitations they include therein.

Amended independent claims 13, 33, 40 and 43, include among other limitations "setting a first breakpoint at a first location in an instruction set in the pipeline," "setting a second breakpoint at a nearest safe point location in the instruction set in the pipeline prior to the first breakpoint location if the first breakpoint location is at an unsafe location in the pipeline," and "simulating instructions of the executing service from the last safe point to a next safe point past the first breakpoint."

Rosenberg does not describe the above limitation. Rosenberg does not disclose "setting a first breakpoint at a first location," and "setting a second breakpoint at a nearest safe point location prior to the first breakpoint location." The cited text in Rosenberg (page 115) describes setting "internal breakpoints and run to the next breakpoint to simulate the single-step functionality." (Page 115, middle of third paragraph). "if the debugger detects the next instruction as a branch instruction it must decode the target of the branch and set a breakpoint there to correctly 'single step' over the branch instruction." (Id., underlining added).

Therefore, the debugger of Rosenberg detects the branches within an instruction set and sets the next breakpoint in the target of the branch, and not in a location "prior to the first

breakpoint location." "Target of the branch" breakpoint, by definition, is clearly in a location ahead of the branch itself (with respect to the program flow), which is not "prior to the first breakpoint location," as required by independent claims 13, 33, 40 and 43.

Consequently, independent claims 13, 33, 40 and 43 are not anticipated by Rosenberg. Dependent claims 14-15, 34-35, 52, and 54 are dependent from independent claims 13, 33, 40 and 43, respectively and therefore include all the limitations of their respective independent claims and additional limitations therein. Accordingly, these claims are also allowable over the cited references, as being dependent from allowable independent claims and for the additional limitations they include therein.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
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